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Jitter – An Introduction

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Abstract: *Serial data systems play an increasingly important role whenever volumes of data are processed or transported. Jitter is a key concern for engineers developing high speed components such as transmitters, receivers and data channels. Serial high speed communication systems need to operate within very tight margins; with data provided extremely fast and with an exceptionally low probability of errors. The challenge for developers is to create high speed systems at very low cost so products can be competitively marketed.*

Discussing the subject matter of jitter completely would exceed the scale of this paper. Instead, it provides a general introduction to jitter, causes and methods of jitter measurements, specifically BER and the eye diagram. It will also talk about examples of standards concerning jitter-tolerance-measurements for serial high speed components and will take a closer look at the test setup for a serial high speed PCI express receiver.

What is Jitter?

"Jitter" is a term used in the digital domain, even if causes and resulting effects are very much of analog nature. Binary information is transmitted as bits in a data stream of random ones and zeros. In an ideal world these bits would be available strictly at a certain time and be present for an exactly predetermined period. Furthermore, they would have uniform high and low levels. Unfortunately, the real world scenario is far from ideal. Designers have to overcome a variety of factors that influence and the transmitted data signal quality and happen to be a source of jitter. Jitter is commonly recognized as a high frequency quantity. Jitter-like be-

havior at frequencies below 10 Hz is called “wander” and “drift” at even lower frequencies. Though they are a concern in large-scale synchronous systems, wander and drift play a negligible role in asynchronous systems because they are easily tracked by clock data recovery units. Asynchronous systems do utilize independent reference clocks for transmitters and receivers. The needed clock frequency in a serial receiver is extracted from the incoming data stream, where bit transitions are utilized to synchronize the phase locked looped VCO of a clock data recovery unit (CDR).

Phase & Amplitude Jitter

Timing variations relative to the ideal transition time are called phase jitter (Fig. 1 top). Signal level variations also occur in digital systems; are called amplitude jitter (Fig. 1 bottom). Because of finite signal transition times, state level variations have an impact on the systems binary state determination. Depending on its originating level just before transition, the slope of the signal reaches the threshold determining the actual bit state somewhat sooner or later. This again has an effect on the “1” or “0” decision period available to the system. Since it is always dependent on the technology standard, there is no universal definition of jitter. The International Telecommunication Union (ITU-I) defines Jitter as:

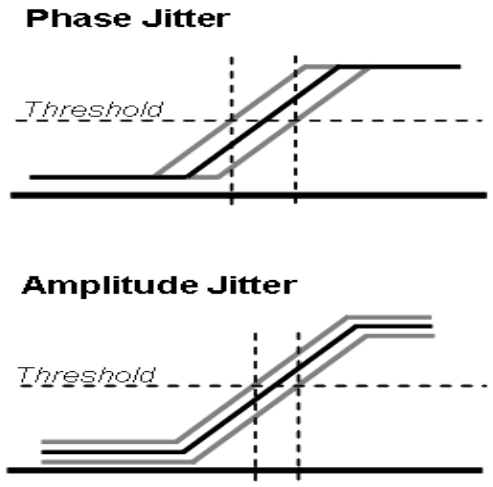

Figure 1. Phase and amplitude jitter influence digital systems and can cause bit errors.

The short-term variation of the significant instants of a digital signal from their ideal positions in time.

Jitter can be bounded or unbounded. The former is related in frequency and magnitude to system events; therefore, bounded jitter is deterministic. This means disabling the source will stop related bounded jitter too. Bounded jitter always has a limited magnitude. An example would be Inter Symbol Interference (ISI): signal transitions cause interference to the neighboring channels, but if the

originating data lines are inactive no interference occurs. Because of the finite energy of originating events, resulting jitter is also finite and always attenuated. Unbounded jitter does not depend on events. System components or external influences can cause it. Most prominent is Random Jitter (RJ), which is caused by white noise prevalent in all active and passive components. Amplifiers and line drivers multiply the energy of noise. By its nature, energy distribution of white noise is Gaussian, so RJ can be described by the probability density function:

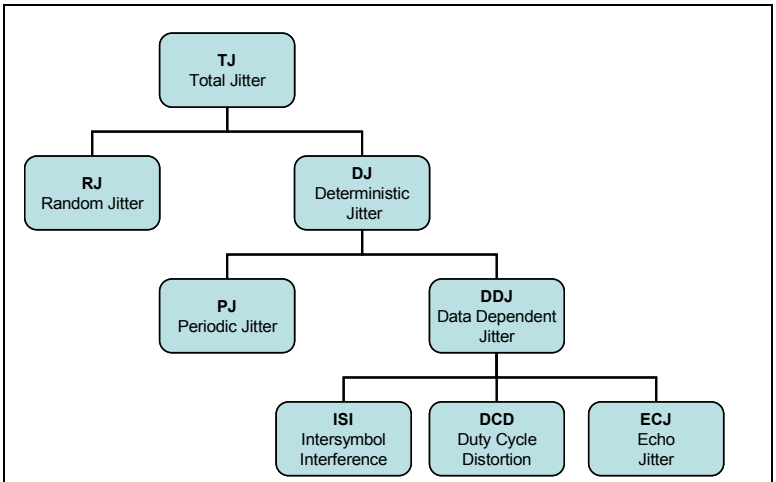

Figure 2. The jitter tree shows types of jitter that can influence high speed serial data systems.

$$\mathrm{PDF}_{RJ}(x) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left(-\frac{(x-\mu)^2}{2\sigma^2}\right)$$

Equation 1

where x is the independent value and σ (sigma) the RMS value and μ (mu) the mean of the distribution. Jitter is defined as deviation from the ideal state, which means it has positive and negative variations relative to the ideal state. For this reason μ in jitter analysis is always 0 and can be omitted. Equation 1 indicates that independently of how large x may become, the probability of certain jitter causing events may become very small, but it will never reach the x-axis. Due to its wide frequency spectrum white noise is very difficult to suppress or attenuate without impacting the actual signal.

System Jitter is caused by a variety of sources, and is either random or deterministic. The latter means that its causes are clearly linked to system events. As described above, such causes could for example be interference with neighboring channels during level transitions or insufficiently filtered switching pulses that are carried over from a switching power supply onto the Vcc network. Table 1 provides a full description of jitter causes.

Jitter Term	Description
TJ Total Jitter	The summation (or convolution) of deterministic and random jitter. Total jitter is the peak to peak value obtained. TJ = DJ + n × RJ where n = number of standard deviations corresponding to the required BER.
RJ Random Jitter	The principal source is Gaussian (white) noise within system components. It interacts with the slew rate of signals and produces timing errors at the switching points.
DJ Deterministic Jitter	Jitter with non-Gaussian probability density function. It is always bounded in amplitude and with specific causes. Sources are imperfections of devices, crosstalk, EMI, grounding problems.
PJ Periodic Jitter	Also called Sinusoidal Jitter due to its sinusoidal form. The source is usually interference form signals related to the data pattern, ground bounce or power supply variations.
DDJ Data dependent Jitter	Consists of Inter Symbol interference (ISI), Duty Cycle distortion (DCD), and Echo Jitter (ECJ). Timing errors vary with data pattern. Primary source are component and system bandwidth limitations. Higher frequency signals have less time to settle than lower frequency ones. This leads to changes in the start conditions for transitions at different frequencies and produces timing errors dependent on the data pattern being applied.
ISI Inter Symbol Interference	Inter symbol interference is the most common form of DDJ. It is usually caused by bandwidth limitations of transmission lines. It affects single bits surrounded by the bit of the opposite state.
DCD Duty Cycle Distortion	Duty Cycle Distortion Jitter is caused when certain bit states have different durations. “1” is always longer than “0” or vice versa. Caused by bias setting, and insufficient VCC supply of a component.
ECJ Echo Jitter	Echo Jitter is caused by component/line mismatch, it depends on the data pattern. Line length influence the magnitude of ECJ as well.

Table 1. Jitter types that can influence serial data systems.

Measuring Jitter: Eye Diagram & BER

How to measure high speed data streams and analyze integrity of the data streams transmitted or received? The prevalent way to conduct this measurement is to determine the Bit Error Rate (BER). A known (pseudo-) random bit stream is injected into the device under test (DUT). The output of the DUT is compared against the known data pattern and possible bit errors are counted:

$$\mathbf{BER} = \mathbf{N_{Err}} \;/\; \mathbf{N_{Bits}}$$

Equation 2

where BER is the measured bit error rate, N_{Err} the number of error bits and N_{Bits} the entire number of compared bits. This requires very sophisticated measurement equipment that allows the comparison of each bit's amplitude and transition timing and offers capabilities to adjust the signal propagation delay that is entailed with the DUT. The ideal condition serves as reference for jitter related measurements and is called unit interval (UI):

1 UI = time period of 1 symbol

Transition time and (differential) amplitude influence the outcome of measurements and determine the binary value of a particular bit. Special BERT testers or oscilloscopes represent the entire data stream through an eye diagram. All measured bits are displayed at the same time. While the measurement technology has to be quite sophisticated due to very high data speeds and relatively low signal levels, the principle of creating an eye diagram is quite simple (Fig. 3). In

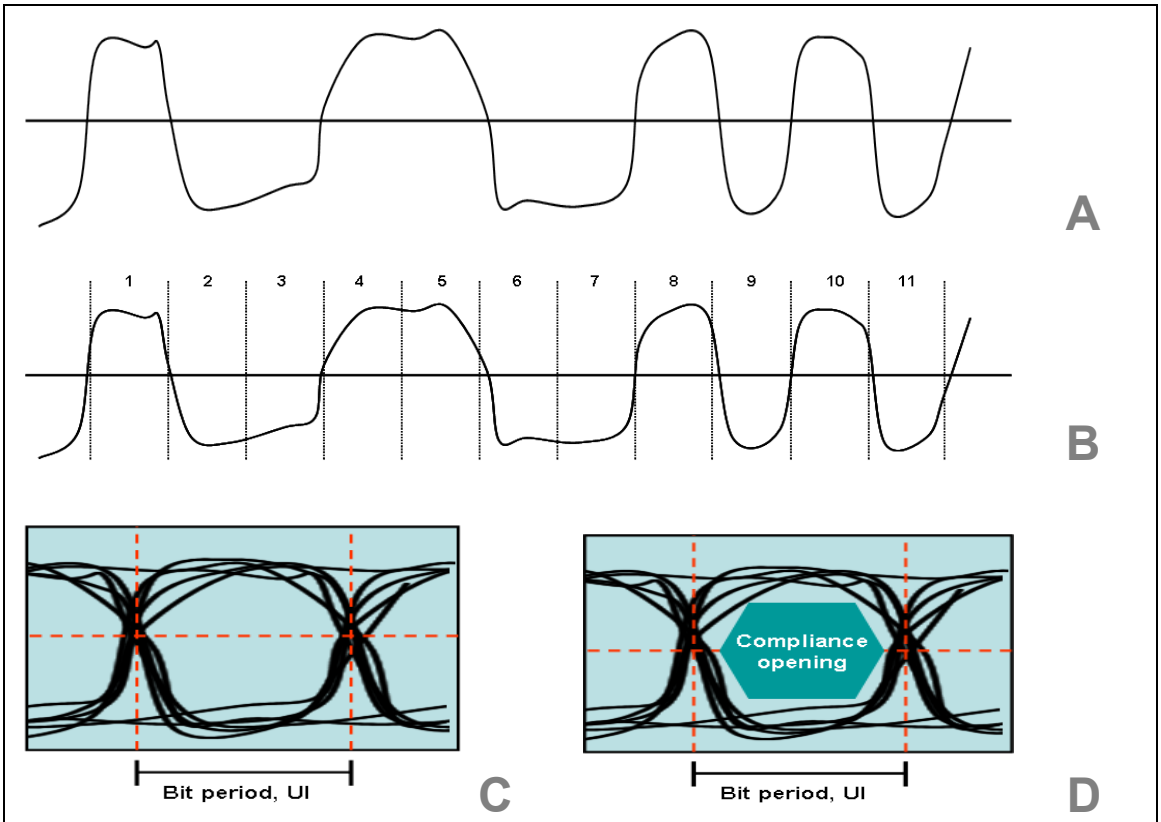

Figure 3. The eye diagram presents the behavior of a very long data stream in a 2UI window. The whole data stream is folded into the window. The eye diagram allows determination of a signal's compliance with requirements defined by the technology standards. Eye diagrams C and D are stretched in the x-axis by a factor of 2.5 for better resolution.

our example, a bit stream (A) is broken in equal increments: I_1 to I_{11} (B), each the size of one bit period, which means per definition 1 UI. To allow detailed analysis of the most important signal parts – the transitions – increments of 2 UI; 0.5 UI pre-transition, 1UI bit sample and 0.5 UI post-transition are recorded and overlaid in a 2 UI wide window. The result is the eye diagram as shown in (Fig. 3 C).

The ideal shape of a data bit would match exactly one unit interval (UI) in both, time and amplitude. Furthermore, under ideal conditions the tolerance margin would be nearly 1UI (–0.5 UI to +0.5 UI relative to the bit center), to recognize signal states properly. The cumulative influence of jitter sources alters signal amplitude and transition timing which reduces the tolerance margin significantly. Compliance opening as depicted in fig. 2 D tells exactly how much signal transitions and levels are allowed to vary from the ideal state before they cause a bit error. Technology standards provide exact descriptions of test setups and measurement margins necessary for meaningful pass / fail decisions. Table 2 shows an excerpt of these requirements for PCIe 2.0, 10Gb Ethernet and SATA II. Some formats allow for more than 50% margin while others are far stricter. The reader may consult the actual technology standards for more comprehensive information. Figure 4 shows the simplified test setup for a PCIe 2.0 jitter compliance test of a serial receiver (DUT). Purpose of this test setup is to expose the DUT to signal conditions that are defined by the standard. Once the DUT passes the compliance test, it is ensured that the hardware will work well with other components that also passed the test. A pattern generator provides a known data stream to the DUT. For synchronous systems, both, DUT and pattern generator are clocked with the same precision clock. Output data of the DUT is compared with the pattern generator for BER analysis. DUT stressing is achieved by varying the signal's amplitude, through different data patterns and generating different data speeds, as seen at the bottom of the pattern generator. The original data stream is additionally modulated in different ways. A variable signal generator with a range from 1.5 to 100 MHz generates PJ conditions, another generator, fixed at 33kHz, serves as spread spectrum clocking simulation. Signal's transition timing is altered through a phase generator and a Gaussian white noise generator that injects RJ with

	Compliance for Eye Opening	Dynamic Amplitude Range	PJ	RJ	ISI
PCIe 2.0	0.4 UI	0.6 Ui	yes	0.16 UI	yes
10 GbE	0.7 UI	no	0.05 to 0.15 UI	no	0.25 UI
SATA II	0.35 UI	no	0.35 UI	0.3 UI	

Table 2. Example (excerpt) of measurement requirements for PCIe 2.0, 10 GBE, and SATA II

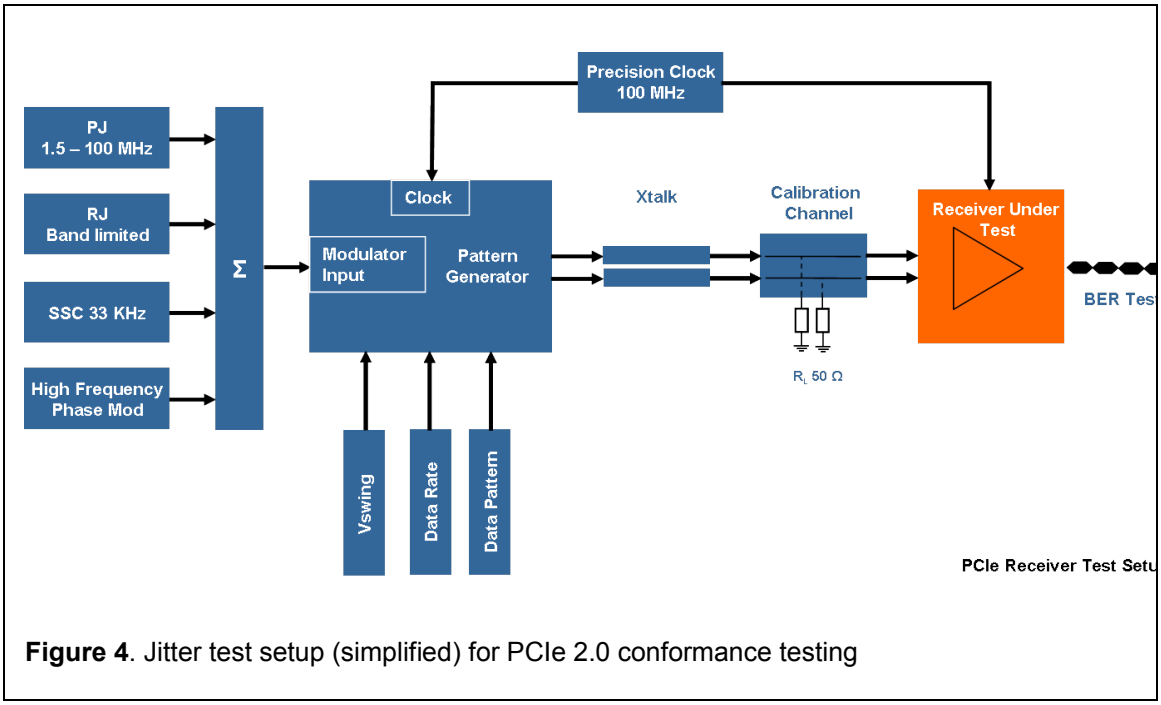

Figure 4. Jitter test setup (simplified) for PCIe 2.0 conformance testing

spectral distribution. Finally ISI is generated through special crosstalk lines at the output of the pattern generator.

Conclusion

This paper introduced different types of jitter: random jitter (RJ), deterministic jitter (DJ) and deterministic jitter's most important sub-classes. Also discussed were the influence of jitter on the signal integrity of high-speed serial data systems and methods of measurement (BER, eye diagram).